**CSE4117 – Microprocessors**



**HOMEWORK-4**

**NAME SURNAME** **STUDENT NUMBER**

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**EXPLANATIONS**

In this homework, firstly we combined the ram in our second homework and the last version of the alu that we designed. Also we added a rom to take the instructions.

The control unit produces **ramEn, r\_w, readRam, writeRam, marEn** in addition to ‘fetch’, ‘decode’ and ‘execute’, then these signals connects to related structures. To produce these signals respectively we implemented a final state machine in the control unit.

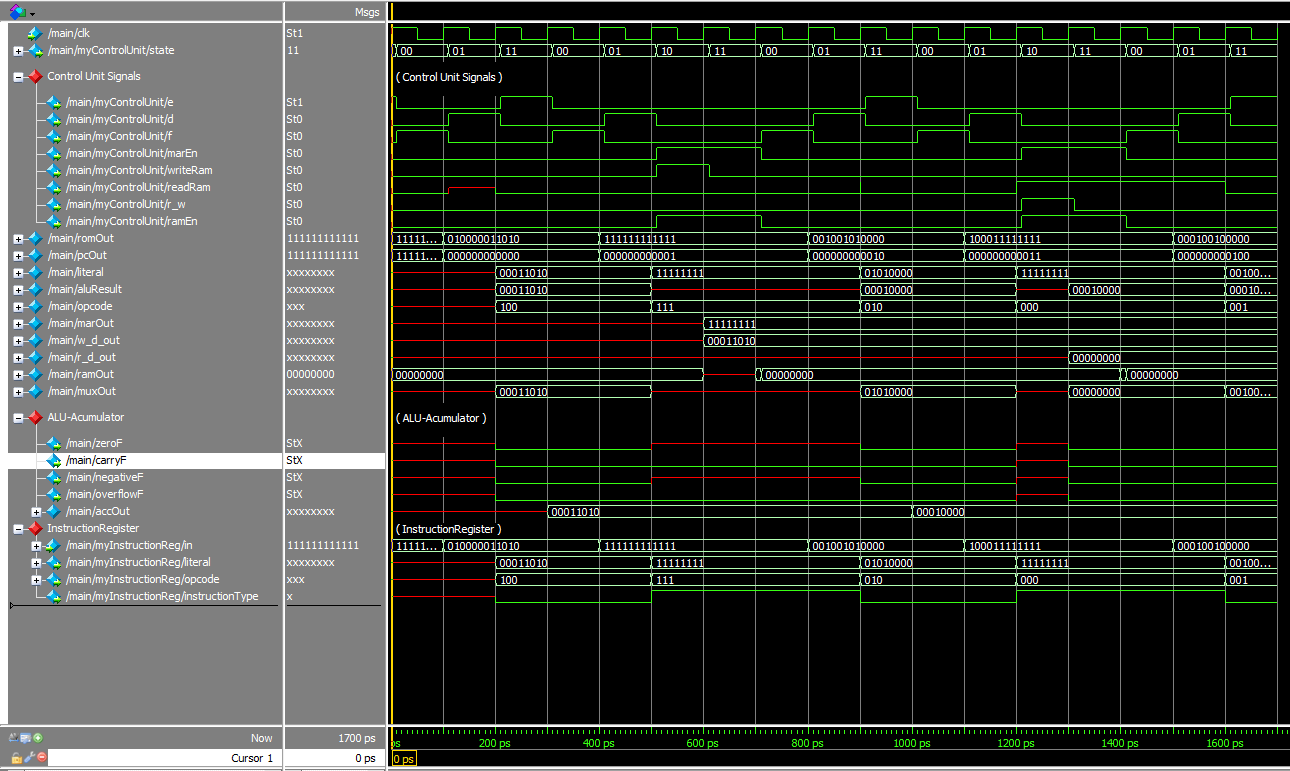
We simulated our model and we obtained partially successful results.

In the simulation below there are five instructions executed which are (1 bit instruction type, 3 bits operation code, 8 bits literal / address):

* MOVA 26 (0 100 00011010) => // Accumulator = 26
* STORER 0xFF (1 111 11111111) => // The value at address 0xFF = 26
* ANDA 80 (0 010 01010000) => // Accumulator = Accumulator & 80
* ADDR 0xFF (1 000 11111111) => // Accumulator = Accumulator + The value at

address 0xFF

* SUBA 32 (0 001 00100000) => // Accumulator = 32 - Accumulator



**OUR SOURCE CODE:**

**Main:**

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| // Aydın DUYGU - 150118981  // Tugay SARICI - 150119829  //-------------------------------------------------------  module onebitsubstractor(input a, input b, input c\_in, output c\_out, output result);  assign c\_out = (~a&b)|(b&c\_in)|(~a&c\_in);  assign result = (a ^ b) ^ c\_in;  endmodule  //-------------------------------------------------------  module twobitsubstractor(input [1:0]a,input [1:0]b, input c\_in, output c\_out, output [1:0] result);  wire cout;  onebitsubstractor s0(a[0],b[0],c\_in,cout,result[0]);  onebitsubstractor s1(a[1],b[1],cout,c\_out,result[1]);  endmodule  //-------------------------------------------------------  module fourbitsubstractor(input [3:0]a,input [3:0]b, input c\_in, output c\_out, output [3:0] result);  wire cout;  twobitsubstractor s0(a[1:0],b[1:0],c\_in,cout,result[1:0]);  twobitsubstractor s1(a[3:2],b[3:2],cout,c\_out,result[3:2]);  endmodule  //-------------------------------------------------------  module eightbitsubstractor(input [7:0]a,input [7:0]b, input c\_in, output c\_out, output [7:0] result);  wire cout;  fourbitsubstractor s0(a[3:0],b[3:0],c\_in,cout,result[3:0]);  fourbitsubstractor s1(a[7:4],b[7:4],cout,c\_out,result[7:4]);  endmodule  //-------------------------------------------------------  module fulladder(  input [7:0] a,  input [7:0] b,  input c\_in,  output reg c\_out,  output reg [7:0] resultFullAdder);    always @(a or b or c\_in)  begin  {c\_out, resultFullAdder} = a+b+c\_in;  end  endmodule  //-------------------------------------------------------  module mux2to1(in0,in1,sel0,out);  input[7:0] in0,in1;  input sel0;  output[7:0] out;  assign out[7] = (in0[7] & ~sel0)|(in1[7] & sel0);  assign out[6] = (in0[6] & ~sel0)|(in1[6] & sel0);  assign out[5] = (in0[5] & ~sel0)|(in1[5] & sel0);  assign out[4] = (in0[4] & ~sel0)|(in1[4] & sel0);  assign out[3] = (in0[3] & ~sel0)|(in1[3] & sel0);  assign out[2] = (in0[2] & ~sel0)|(in1[2] & sel0);  assign out[1] = (in0[1] & ~sel0)|(in1[1] & sel0);  assign out[0] = (in0[0] & ~sel0)|(in1[0] & sel0);  endmodule  //-------------------------------------------------------  module mux4to1(in0,in1,in2,in3,sel0,sel1,out);  input[7:0] in0,in1,in2,in3;  input sel0,sel1;  output[7:0] out;  wire[7:0] w1,w2;  mux2to1 m1(in0,in1,sel0,w1);  mux2to1 m2(in2,in3,sel0,w2);  mux2to1 m3(w1,w2,sel1,out);  endmodule  //-------------------------------------------------------  module mux\_8to1(in0,in1,in2,in3,in4,in5,in6,in7,sel0,sel1,sel2,out);  input[7:0] in0,in1,in2,in3,in4,in5,in6,in7;  input sel0,sel1,sel2;  output[7:0] out;  wire[7:0] w1,w2;  mux4to1 m1(in0,in1,in2,in3,sel0,sel1,w1);  mux4to1 m2(in4,in5,in6,in7,sel0,sel1,w2);  mux2to1 m3(w1,w2,sel2,out);  endmodule  //-------------------------------------------------------  module alu(a, b, opSel, zeroF, carryF, negativeF, overflowF, result);  input [7:0] a, b;  input [2:0] opSel;  output zeroF, negativeF, carryF, overflowF;  output [7:0] result;  wire [7:0] result0, result1, result2, result3, result4, result5, result6, result7;  wire carryFS, carryFA;  fulladder f(a, b, 0, carryFA, result0);  eightbitsubstractor s(a, b, 0, carryFS, result1);  assign result2 = a & b;  assign result3 = a | b;  assign result4 = a;  assign result5 = b << 1;  assign result6 = b >> 1;  assign result7 = a ^ b;  mux\_8to1 mux1(result0, result1,result2, result3, result4, result5, result6, result7, opSel[0], opSel[1], opSel[2], result);  assign zeroF = ~(result[7] | result[6] | result[5] | result[4] | result[3] | result[2] | result[1] | result[0]);  assign negativeF = result[7] ;  assign overflowF = (((~a[7] & ~b[7] & result[7]) | (a[7] & b[7] & ~result[7])) & (~opSel[0] & ~opSel[1] & ~opSel[2])) |  (((~a[7] & b[7] & result[7]) | (a[7] & ~b[7] & ~result[7])) & (opSel[0] & ~opSel[1] & ~opSel[2]));    assign carryF = (~opSel[0] & ~opSel[1] & ~opSel[2] & carryFA) | (opSel[0] & ~opSel[1] & ~opSel[2] & carryFS);    endmodule  //-------------------------------------------------------  // FIRST ASSIGNMENT UNTIL HERE  //-------------------------------------------------------  //-------------------------------------------------------  module accumulator(accIn, e, clk, accOut);  input [7:0] accIn;  input e, clk;  output [7:0] accOut;  reg [7:0] accOut;  always @ (posedge clk) begin  if(e == 1)  accOut = accIn;  end  endmodule  //-------------------------------------------------------  module instruction\_register(in, d, clk, literal, opcode,instructionType);  // instructionType: 1bit + opcode: 3 bits + value: 8 bits  input [11:0] in;  input d, clk;  output [7:0] literal;  reg [7:0] literal;  output [2:0] opcode;  reg [2:0] opcode;  output instructionType;  reg instructionType;  always @ (posedge clk)  begin  if (d == 1) begin  literal[0] <= in[0];  literal[1] <= in[1];  literal[2] <= in[2];  literal[3] <= in[3];  literal[4] <= in[4];  literal[5] <= in[5];  literal[6] <= in[6];  literal[7] <= in[7];  opcode[0] <= in[8];  opcode[1] <= in[9];  opcode[2] <= in[10];  instructionType<=in[11];  end  end  endmodule  //-------------------------------------------------------  module controlUnit(instructionTypeInput,opcode,clk,state,e,d,f,marEn,writeRam,readRam,r\_w,ramEn);  input instructionTypeInput;  input [2:0] opcode;  input clk;  output e,d,f,marEn,writeRam,readRam,r\_w,ramEn;  output [1:0] state;  reg [1:0] state = 2'b11;  reg firstRun=1;  reg instructionType;  assign f=(~state[1])&(~state[0]);  assign d=(~state[1])&(state[0]);  assign e=(state[1])&(state[0])&(~instructionType);  assign marEn=((state[1])&(state[0])&instructionType)|(state[1]&~state[0]);  assign writeRam=(instructionType&(opcode[2]&opcode[1]&opcode[0])&((state[1])&(~state[0])));  assign readRam=(instructionType&(~(opcode[2]&opcode[1]&opcode[0])));  assign r\_w=(instructionType&(~(opcode[2]&opcode[1]&opcode[0]))&((state[1])&(~state[0])));  assign ramEn=((state[1])&(state[0])&instructionType)|(state[1]&~state[0]);  initial begin  if(firstRun==1) instructionType<=0;      else instructionType<=instructionTypeInput;  end  always@(\*) begin  if(~state[1]&state[0])begin  firstRun<=0;  instructionType<=instructionTypeInput;  end    end  always @ (posedge clk)begin    #10  state[0]<=(~state[0]&~state[1])|(state[0]&~state[1]&~instructionType)|(instructionType&state[1]&~state[0]);  state[1]<=(~state[1]&state[0])|(instructionType&state[1]&~state[0]);    end  endmodule  //-------------------------------------------------------  module programCounter(clk,f,out);  input clk,f;  output[11:0] out;  reg[11:0] out=12'b111111111111;  always @ (posedge clk)    begin  if(f==1) begin  out=out+1;  end  end  endmodule  //-------------------------------------------------------  module mar(clk, in, out, en);  input clk,en;  input [7:0] in;  output [7:0] out;  reg [7:0] out;  always @ (posedge clk)    begin  if(en==1)out<=in;  end    endmodule  //-------------------------------------------------------  module w\_d (clk, in, out, en);  input clk,en;  input [7:0] in;  output [7:0] out;  reg [7:0] out;  always @ (posedge clk)    begin  if(en==1)out<=in;  end    endmodule  //-------------------------------------------------------  module r\_d (clk, in, out, en);  input clk,en;  input [7:0] in;  output [7:0] out;  reg [7:0] out;  always @ (posedge clk)begin  if(en==1)out<=in;  end    endmodule  //-------------------------------------------------------  module main(clk,zeroF, carryF, negativeF, overflowF);  input clk;  wire [11:0] romOut,pcOut;  wire [7:0] literal,aluResult;  wire instructionType;  wire [2:0] opcode;  wire e,d,f;  wire [7:0] marOut,w\_d\_out,r\_d\_out,ramOut,muxOut;  wire marEn,readRam,writeRam,r\_w,ramEn;  output zeroF, carryF, negativeF, overflowF;  wire [7:0] accOut;  controlUnit myControlUnit(instructionType,opcode,clk,state,e,d,f,marEn,writeRam,readRam,r\_w,ramEn);  programCounter pc(clk,f,pcOut);  rom myrom(pcOut,romOut);  instruction\_register myInstructionReg(romOut,d, clk, literal, opcode,instructionType);  mar mymar(clk,literal,marOut,marEn);  w\_d mywd(clk,accOut,w\_d\_out,writeRam);  ram myram(w\_d\_out,r\_w,clk,ramOut,marOut,ramEn);  r\_d myrd(clk,ramOut,r\_d\_out,readRam);  mux2to1 mymux(literal,r\_d\_out,instructionType,muxOut);  alu myALU(muxOut, accOut, opcode, zeroF, carryF, negativeF, overflowF, aluResult);  accumulator myAccumulator(aluResult, e, clk, accOut);  endmodule |

**RAM:**

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| module dflipflop(d, q, clk);  input d, clk;  output q;  reg q;  always @ (posedge clk)  begin  q <= d;  end  endmodule  //------------------------------------------------------------  module binarycell(sel, dataIn, rw, clk, dataOut);  input dataIn, clk, sel, rw;  output dataOut;  wire w1, w2, q;  reg dataOut;  assign w1 = (sel & ~rw);  assign w2 = w1 ? dataIn : dataOut;  dflipflop binflop(w2, q, clk);  always @ ( \* ) begin  dataOut <= (sel & q);  end  endmodule  //------------------------------------------------------------  module decoder\_4to16(a1, a2, a3, a4, e, dOut);  input a1, a2, a3, a4, e;  output [15:0] dOut;  assign dOut[0] = (~a1) & (~a2) &(~a3) & (~a4) & (e);  assign dOut[1] = (~a1) & (~a2) &(~a3) & (a4) & (e);  assign dOut[2] = (~a1) & (~a2) &(a3) & (~a4) & (e);  assign dOut[3] = (~a1) & (~a2) &(a3) & (a4) & (e);  assign dOut[4] = (~a1) & (a2) &(~a3) & (~a4) & (e);  assign dOut[5] = (~a1) & (a2) &(~a3) & (a4) & (e);  assign dOut[6] = (~a1) & (a2) &(a3) & (~a4) & (e);  assign dOut[7] = (~a1) & (a2) &(a3) & (a4) & (e);  assign dOut[8] = (a1) & (~a2) &(~a3) & (~a4) & (e);  assign dOut[9] = (a1) & (~a2) &(~a3) & (a4) & (e);  assign dOut[10] = (a1) & (~a2) &(a3) & (~a4) & (e);  assign dOut[11] = (a1) & (~a2) &(a3) & (a4) & (e);  assign dOut[12] = (a1) & (a2) &(~a3) & (~a4) & (e);  assign dOut[13] = (a1) & (a2) &(~a3) & (a4) & (e);  assign dOut[14] = (a1) & (a2) &(a3) & (~a4) & (e);  assign dOut[15] = (a1) & (a2) &(a3) & (a4) & (e);  endmodule  //------------------------------------------------------------  module RamPart(dOut, data, rw, clk, out);  input [15:0] dOut;  input [7:0] data;  input rw, clk;  output [7:0] out;  wire out0000\_1 , out0001\_1 , out0010\_1 , out0011\_1 , out0100\_1 , out0101\_1 , out0110\_1 , out0111\_1 , out1000\_1 , out1001\_1 , out1010\_1 , out1011\_1 , out1100\_1 , out1101\_1 , out1110\_1 , out1111\_1;  wire out0000\_2 , out0001\_2 , out0010\_2 , out0011\_2 , out0100\_2 , out0101\_2 , out0110\_2 , out0111\_2 , out1000\_2 , out1001\_2 , out1010\_2 , out1011\_2 , out1100\_2 , out1101\_2 , out1110\_2 , out1111\_2;  wire out0000\_3 , out0001\_3 , out0010\_3 , out0011\_3 , out0100\_3 , out0101\_3 , out0110\_3 , out0111\_3 , out1000\_3 , out1001\_3 , out1010\_3 , out1011\_3 , out1100\_3 , out1101\_3 , out1110\_3 , out1111\_3;  wire out0000\_4 , out0001\_4 , out0010\_4 , out0011\_4 , out0100\_4 , out0101\_4 , out0110\_4 , out0111\_4 , out1000\_4 , out1001\_4 , out1010\_4 , out1011\_4 , out1100\_4 , out1101\_4 , out1110\_4 , out1111\_4;  wire out0000\_5 , out0001\_5 , out0010\_5 , out0011\_5 , out0100\_5 , out0101\_5 , out0110\_5 , out0111\_5 , out1000\_5 , out1001\_5 , out1010\_5 , out1011\_5 , out1100\_5 , out1101\_5 , out1110\_5 , out1111\_5;  wire out0000\_6 , out0001\_6 , out0010\_6 , out0011\_6 , out0100\_6 , out0101\_6 , out0110\_6 , out0111\_6 , out1000\_6 , out1001\_6 , out1010\_6 , out1011\_6 , out1100\_6 , out1101\_6 , out1110\_6 , out1111\_6;  wire out0000\_7 , out0001\_7 , out0010\_7 , out0011\_7 , out0100\_7 , out0101\_7 , out0110\_7 , out0111\_7 , out1000\_7 , out1001\_7 , out1010\_7 , out1011\_7 , out1100\_7 , out1101\_7 , out1110\_7 , out1111\_7;  wire out0000\_8 , out0001\_8 , out0010\_8 , out0011\_8 , out0100\_8 , out0101\_8 , out0110\_8 , out0111\_8 , out1000\_8 , out1001\_8 , out1010\_8 , out1011\_8 , out1100\_8 , out1101\_8 , out1110\_8 , out1111\_8;    //module binarycell(en,data,rw,clk,out);  binarycell cell\_0000\_1(dOut[0],data[0],rw,clk,out0000\_1);  binarycell cell\_0001\_1(dOut[1],data[0],rw,clk,out0001\_1);  binarycell cell\_0010\_1(dOut[2],data[0],rw,clk,out0010\_1);  binarycell cell\_0011\_1(dOut[3],data[0],rw,clk,out0011\_1);  binarycell cell\_0100\_1(dOut[4],data[0],rw,clk,out0100\_1);  binarycell cell\_0101\_1(dOut[5],data[0],rw,clk,out0101\_1);  binarycell cell\_0110\_1(dOut[6],data[0],rw,clk,out0110\_1);  binarycell cell\_0111\_1(dOut[7],data[0],rw,clk,out0111\_1);  binarycell cell\_1000\_1(dOut[8],data[0],rw,clk,out1000\_1);  binarycell cell\_1001\_1(dOut[9],data[0],rw,clk,out1001\_1);  binarycell cell\_1010\_1(dOut[10],data[0],rw,clk,out1010\_1);  binarycell cell\_1011\_1(dOut[11],data[0],rw,clk,out1011\_1);  binarycell cell\_1100\_1(dOut[12],data[0],rw,clk,out1100\_1);  binarycell cell\_1101\_1(dOut[13],data[0],rw,clk,out1101\_1);  binarycell cell\_1110\_1(dOut[14],data[0],rw,clk,out1110\_1);  binarycell cell\_1111\_1(dOut[15],data[0],rw,clk,out1111\_1);  binarycell cell\_0000\_2(dOut[0],data[1],rw,clk,out0000\_2);  binarycell cell\_0001\_2(dOut[1],data[1],rw,clk,out0001\_2);  binarycell cell\_0010\_2(dOut[2],data[1],rw,clk,out0010\_2);  binarycell cell\_0011\_2(dOut[3],data[1],rw,clk,out0011\_2);  binarycell cell\_0100\_2(dOut[4],data[1],rw,clk,out0100\_2);  binarycell cell\_0101\_2(dOut[5],data[1],rw,clk,out0101\_2);  binarycell cell\_0110\_2(dOut[6],data[1],rw,clk,out0110\_2);  binarycell cell\_0111\_2(dOut[7],data[1],rw,clk,out0111\_2);  binarycell cell\_1000\_2(dOut[8],data[1],rw,clk,out1000\_2);  binarycell cell\_1001\_2(dOut[9],data[1],rw,clk,out1001\_2);  binarycell cell\_1010\_2(dOut[10],data[1],rw,clk,out1010\_2);  binarycell cell\_1011\_2(dOut[11],data[1],rw,clk,out1011\_2);  binarycell cell\_1100\_2(dOut[12],data[1],rw,clk,out1100\_2);  binarycell cell\_1101\_2(dOut[13],data[1],rw,clk,out1101\_2);  binarycell cell\_1110\_2(dOut[14],data[1],rw,clk,out1110\_2);  binarycell cell\_1111\_2(dOut[15],data[1],rw,clk,out1111\_2);  binarycell cell\_0000\_3(dOut[0],data[2],rw,clk,out0000\_3);  binarycell cell\_0001\_3(dOut[1],data[2],rw,clk,out0001\_3);  binarycell cell\_0010\_3(dOut[2],data[2],rw,clk,out0010\_3);  binarycell cell\_0011\_3(dOut[3],data[2],rw,clk,out0011\_3);  binarycell cell\_0100\_3(dOut[4],data[2],rw,clk,out0100\_3);  binarycell cell\_0101\_3(dOut[5],data[2],rw,clk,out0101\_3);  binarycell cell\_0110\_3(dOut[6],data[2],rw,clk,out0110\_3);  binarycell cell\_0111\_3(dOut[7],data[2],rw,clk,out0111\_3);  binarycell cell\_1000\_3(dOut[8],data[2],rw,clk,out1000\_3);  binarycell cell\_1001\_3(dOut[9],data[2],rw,clk,out1001\_3);  binarycell cell\_1010\_3(dOut[10],data[2],rw,clk,out1010\_3);  binarycell cell\_1011\_3(dOut[11],data[2],rw,clk,out1011\_3);  binarycell cell\_1100\_3(dOut[12],data[2],rw,clk,out1100\_3);  binarycell cell\_1101\_3(dOut[13],data[2],rw,clk,out1101\_3);  binarycell cell\_1110\_3(dOut[14],data[2],rw,clk,out1110\_3);  binarycell cell\_1111\_3(dOut[15],data[2],rw,clk,out1111\_3);  binarycell cell\_0000\_4(dOut[0],data[3],rw,clk,out0000\_4);  binarycell cell\_0001\_4(dOut[1],data[3],rw,clk,out0001\_4);  binarycell cell\_0010\_4(dOut[2],data[3],rw,clk,out0010\_4);  binarycell cell\_0011\_4(dOut[3],data[3],rw,clk,out0011\_4);  binarycell cell\_0100\_4(dOut[4],data[3],rw,clk,out0100\_4);  binarycell cell\_0101\_4(dOut[5],data[3],rw,clk,out0101\_4);  binarycell cell\_0110\_4(dOut[6],data[3],rw,clk,out0110\_4);  binarycell cell\_0111\_4(dOut[7],data[3],rw,clk,out0111\_4);  binarycell cell\_1000\_4(dOut[8],data[3],rw,clk,out1000\_4);  binarycell cell\_1001\_4(dOut[9],data[3],rw,clk,out1001\_4);  binarycell cell\_1010\_4(dOut[10],data[3],rw,clk,out1010\_4);  binarycell cell\_1011\_4(dOut[11],data[3],rw,clk,out1011\_4);  binarycell cell\_1100\_4(dOut[12],data[3],rw,clk,out1100\_4);  binarycell cell\_1101\_4(dOut[13],data[3],rw,clk,out1101\_4);  binarycell cell\_1110\_4(dOut[14],data[3],rw,clk,out1110\_4);  binarycell cell\_1111\_4(dOut[15],data[3],rw,clk,out1111\_4);  binarycell cell\_0000\_5(dOut[0],data[4],rw,clk,out0000\_5);  binarycell cell\_0001\_5(dOut[1],data[4],rw,clk,out0001\_5);  binarycell cell\_0010\_5(dOut[2],data[4],rw,clk,out0010\_5);  binarycell cell\_0011\_5(dOut[3],data[4],rw,clk,out0011\_5);  binarycell cell\_0100\_5(dOut[4],data[4],rw,clk,out0100\_5);  binarycell cell\_0101\_5(dOut[5],data[4],rw,clk,out0101\_5);  binarycell cell\_0110\_5(dOut[6],data[4],rw,clk,out0110\_5);  binarycell cell\_0111\_5(dOut[7],data[4],rw,clk,out0111\_5);  binarycell cell\_1000\_5(dOut[8],data[4],rw,clk,out1000\_5);  binarycell cell\_1001\_5(dOut[9],data[4],rw,clk,out1001\_5);  binarycell cell\_1010\_5(dOut[10],data[4],rw,clk,out1010\_5);  binarycell cell\_1011\_5(dOut[11],data[4],rw,clk,out1011\_5);  binarycell cell\_1100\_5(dOut[12],data[4],rw,clk,out1100\_5);  binarycell cell\_1101\_5(dOut[13],data[4],rw,clk,out1101\_5);  binarycell cell\_1110\_5(dOut[14],data[4],rw,clk,out1110\_5);  binarycell cell\_1111\_5(dOut[15],data[4],rw,clk,out1111\_5);  binarycell cell\_0000\_6(dOut[0],data[5],rw,clk,out0000\_6);  binarycell cell\_0001\_6(dOut[1],data[5],rw,clk,out0001\_6);  binarycell cell\_0010\_6(dOut[2],data[5],rw,clk,out0010\_6);  binarycell cell\_0011\_6(dOut[3],data[5],rw,clk,out0011\_6);  binarycell cell\_0100\_6(dOut[4],data[5],rw,clk,out0100\_6);  binarycell cell\_0101\_6(dOut[5],data[5],rw,clk,out0101\_6);  binarycell cell\_0110\_6(dOut[6],data[5],rw,clk,out0110\_6);  binarycell cell\_0111\_6(dOut[7],data[5],rw,clk,out0111\_6);  binarycell cell\_1000\_6(dOut[8],data[5],rw,clk,out1000\_6);  binarycell cell\_1001\_6(dOut[9],data[5],rw,clk,out1001\_6);  binarycell cell\_1010\_6(dOut[10],data[5],rw,clk,out1010\_6);  binarycell cell\_1011\_6(dOut[11],data[5],rw,clk,out1011\_6);  binarycell cell\_1100\_6(dOut[12],data[5],rw,clk,out1100\_6);  binarycell cell\_1101\_6(dOut[13],data[5],rw,clk,out1101\_6);  binarycell cell\_1110\_6(dOut[14],data[5],rw,clk,out1110\_6);  binarycell cell\_1111\_6(dOut[15],data[5],rw,clk,out1111\_6);  binarycell cell\_0000\_7(dOut[0],data[6],rw,clk,out0000\_7);  binarycell cell\_0001\_7(dOut[1],data[6],rw,clk,out0001\_7);  binarycell cell\_0010\_7(dOut[2],data[6],rw,clk,out0010\_7);  binarycell cell\_0011\_7(dOut[3],data[6],rw,clk,out0011\_7);  binarycell cell\_0100\_7(dOut[4],data[6],rw,clk,out0100\_7);  binarycell cell\_0101\_7(dOut[5],data[6],rw,clk,out0101\_7);  binarycell cell\_0110\_7(dOut[6],data[6],rw,clk,out0110\_7);  binarycell cell\_0111\_7(dOut[7],data[6],rw,clk,out0111\_7);  binarycell cell\_1000\_7(dOut[8],data[6],rw,clk,out1000\_7);  binarycell cell\_1001\_7(dOut[9],data[6],rw,clk,out1001\_7);  binarycell cell\_1010\_7(dOut[10],data[6],rw,clk,out1010\_7);  binarycell cell\_1011\_7(dOut[11],data[6],rw,clk,out1011\_7);  binarycell cell\_1100\_7(dOut[12],data[6],rw,clk,out1100\_7);  binarycell cell\_1101\_7(dOut[13],data[6],rw,clk,out1101\_7);  binarycell cell\_1110\_7(dOut[14],data[6],rw,clk,out1110\_7);  binarycell cell\_1111\_7(dOut[15],data[6],rw,clk,out1111\_7);  binarycell cell\_0000\_8(dOut[0],data[7],rw,clk,out0000\_8);  binarycell cell\_0001\_8(dOut[1],data[7],rw,clk,out0001\_8);  binarycell cell\_0010\_8(dOut[2],data[7],rw,clk,out0010\_8);  binarycell cell\_0011\_8(dOut[3],data[7],rw,clk,out0011\_8);  binarycell cell\_0100\_8(dOut[4],data[7],rw,clk,out0100\_8);  binarycell cell\_0101\_8(dOut[5],data[7],rw,clk,out0101\_8);  binarycell cell\_0110\_8(dOut[6],data[7],rw,clk,out0110\_8);  binarycell cell\_0111\_8(dOut[7],data[7],rw,clk,out0111\_8);  binarycell cell\_1000\_8(dOut[8],data[7],rw,clk,out1000\_8);  binarycell cell\_1001\_8(dOut[9],data[7],rw,clk,out1001\_8);  binarycell cell\_1010\_8(dOut[10],data[7],rw,clk,out1010\_8);  binarycell cell\_1011\_8(dOut[11],data[7],rw,clk,out1011\_8);  binarycell cell\_1100\_8(dOut[12],data[7],rw,clk,out1100\_8);  binarycell cell\_1101\_8(dOut[13],data[7],rw,clk,out1101\_8);  binarycell cell\_1110\_8(dOut[14],data[7],rw,clk,out1110\_8);  binarycell cell\_1111\_8(dOut[15],data[7],rw,clk,out1111\_8);  assign out[0] = out0000\_1 || out0001\_1 || out0010\_1 || out0011\_1 || out0100\_1 || out0101\_1 || out0110\_1 || out0111\_1 || out1000\_1 || out1001\_1 || out1010\_1 || out1011\_1 || out1100\_1 || out1101\_1 || out1110\_1 || out1111\_1;  assign out[1] = out0000\_2 || out0001\_2 || out0010\_2 || out0011\_2 || out0100\_2 || out0101\_2 || out0110\_2 || out0111\_2 || out1000\_2 || out1001\_2 || out1010\_2 || out1011\_2 || out1100\_2 || out1101\_2 || out1110\_2 || out1111\_2;  assign out[2] = out0000\_3 || out0001\_3 || out0010\_3 || out0011\_3 || out0100\_3 || out0101\_3 || out0110\_3 || out0111\_3 || out1000\_3 || out1001\_3 || out1010\_3 || out1011\_3 || out1100\_3 || out1101\_3 || out1110\_3 || out1111\_3;  assign out[3] = out0000\_4 || out0001\_4 || out0010\_4 || out0011\_4 || out0100\_4 || out0101\_4 || out0110\_4 || out0111\_4 || out1000\_4 || out1001\_4 || out1010\_4 || out1011\_4 || out1100\_4 || out1101\_4 || out1110\_4 || out1111\_4;  assign out[4] = out0000\_5 || out0001\_5 || out0010\_5 || out0011\_5 || out0100\_5 || out0101\_5 || out0110\_5 || out0111\_5 || out1000\_5 || out1001\_5 || out1010\_5 || out1011\_5 || out1100\_5 || out1101\_5 || out1110\_5 || out1111\_5;  assign out[5] = out0000\_6 || out0001\_6 || out0010\_6 || out0011\_6 || out0100\_6 || out0101\_6 || out0110\_6 || out0111\_6 || out1000\_6 || out1001\_6 || out1010\_6 || out1011\_6 || out1100\_6 || out1101\_6 || out1110\_6 || out1111\_6;  assign out[6] = out0000\_7 || out0001\_7 || out0010\_7 || out0011\_7 || out0100\_7 || out0101\_7 || out0110\_7 || out0111\_7 || out1000\_7 || out1001\_7 || out1010\_7 || out1011\_7 || out1100\_7 || out1101\_7 || out1110\_7 || out1111\_7;  assign out[7] = out0000\_8 || out0001\_8 || out0010\_8 || out0011\_8 || out0100\_8 || out0101\_8 || out0110\_8 || out0111\_8 || out1000\_8 || out1001\_8 || out1010\_8 || out1011\_8 || out1100\_8 || out1101\_8 || out1110\_8 || out1111\_8;  endmodule  //------------------------------------------------------------  module ram(data, rw, clk, out, addr, EN);  input [7:0] addr;  input rw, clk, EN;  input[7:0] data;  output[7:0] out;  wire [7:0] out1, out2,out3,out4,out5,out6,out7,out8,out9,out10,out11,out12,out13,out14,out15,out16;  wire [15:0] dOut;  wire [15:0] d1\_Out;  wire [15:0] d2\_Out;  wire [15:0] d3\_Out;  wire [15:0] d4\_Out;  wire [15:0] d5\_Out;  wire [15:0] d6\_Out;  wire [15:0] d7\_Out;  wire [15:0] d8\_Out;  wire [15:0] d9\_Out;  wire [15:0] d10\_Out;  wire [15:0] d11\_Out;  wire [15:0] d12\_Out;  wire [15:0] d13\_Out;  wire [15:0] d14\_Out;  wire [15:0] d15\_Out;  wire [15:0] d16\_Out;  decoder\_4to16 decoder(addr[7], addr[6], addr[5], addr[4], EN, dOut);  decoder\_4to16 decoder1(addr[3], addr[2], addr[1], addr[0], dOut[0], d1\_Out);  decoder\_4to16 decoder2(addr[3], addr[2], addr[1], addr[0], dOut[1], d2\_Out);  decoder\_4to16 decoder3(addr[3], addr[2], addr[1], addr[0], dOut[2], d3\_Out);  decoder\_4to16 decoder4(addr[3], addr[2], addr[1], addr[0], dOut[3], d4\_Out);  decoder\_4to16 decoder5(addr[3], addr[2], addr[1], addr[0], dOut[4], d5\_Out);  decoder\_4to16 decoder6(addr[3], addr[2], addr[1], addr[0], dOut[5], d6\_Out);  decoder\_4to16 decoder7(addr[3], addr[2], addr[1], addr[0], dOut[6], d7\_Out);  decoder\_4to16 decoder8(addr[3], addr[2], addr[1], addr[0], dOut[7], d8\_Out);  decoder\_4to16 decoder9(addr[3], addr[2], addr[1], addr[0], dOut[8], d9\_Out);  decoder\_4to16 decoder10(addr[3], addr[2], addr[1], addr[0], dOut[9], d10\_Out);  decoder\_4to16 decoder11(addr[3], addr[2], addr[1], addr[0], dOut[10],d11\_Out);  decoder\_4to16 decoder12(addr[3], addr[2], addr[1], addr[0], dOut[11],d12\_Out);  decoder\_4to16 decoder13(addr[3], addr[2], addr[1], addr[0], dOut[12],d13\_Out);  decoder\_4to16 decoder14(addr[3], addr[2], addr[1], addr[0], dOut[13],d14\_Out);  decoder\_4to16 decoder15(addr[3], addr[2], addr[1], addr[0], dOut[14],d15\_Out);  decoder\_4to16 decoder16(addr[3], addr[2], addr[1], addr[0], dOut[15],d16\_Out);  RamPart h1(d1\_Out, data, rw, clk, out1);  RamPart h2(d2\_Out, data, rw, clk, out2);  RamPart h3(d3\_Out, data, rw, clk, out3);  RamPart h4(d4\_Out, data, rw, clk, out4);  RamPart h5(d5\_Out, data, rw, clk, out5);  RamPart h6(d6\_Out, data, rw, clk, out6);  RamPart h7(d7\_Out, data, rw, clk, out7);  RamPart h8(d8\_Out, data, rw, clk, out8);  RamPart h9(d9\_Out, data, rw, clk, out9);  RamPart h10(d10\_Out, data, rw, clk, out10);  RamPart h11(d11\_Out, data, rw, clk, out11);  RamPart h12(d12\_Out, data, rw, clk, out12);  RamPart h13(d13\_Out, data, rw, clk, out13);  RamPart h14(d14\_Out, data, rw, clk, out14);  RamPart h15(d15\_Out, data, rw, clk, out15);  RamPart h16(d16\_Out, data, rw, clk, out16);  assign out = out1 | out2 | out3 | out4 | out5 | out6 | out7 | out8 | out9 | out10 | out11 | out12 | out13 | out14 | out15 | out16;  endmodule |

**ROM:**

|  |
| --- |
| module rom(addr,out);  input[11:0] addr;  output [11:0] out;  reg[11:0] out;  always@ (\*) begin  case(addr)    12'b000000000000 : out= 12'b010000011010;  12'b000000000001 : out= 12'b111111111111;  12'b000000000010 : out= 12'b001001010000;  12'b000000000011 : out= 12'b100011111111;  12'b000000000100 : out= 12'b000100100000;  12'b000000000101 : out= 12'b011101001011;  12'b000000000110 : out= 12'b111110100010;  12'b000000000111 : out= 12'b110011111111;  12'b000000001000 : out= 12'b101110100010;  12'b000000001001 : out= 12'b100111111111;  12'b000000001010 : out= 12'b111100001000;  12'b000000001011 : out= 12'b010000000010;  12'b000000001100 : out= 12'b111100001111;  12'b000000001101 : out= 12'b110000001000;  12'b000000001110 : out= 12'b111000001111;  12'b000000001111 : out= 12'b010100000011;  12'b000000010000 : out= 12'b001101111111;  12'b000000010001 : out= 12'b011000000100;  12'b000000010010 : out= 12'b111101100001;  12'b000000010011 : out= 12'b010000000111;  12'b000000010100 : out= 12'b101001100001;  12'b000000010101 : out= 12'b110100001111;  12'b000000010110 : out= 12'b000000110000;  // all operations were used  //------------------------------------------  12'b000000010111 : out= 12'b000000010111;  12'b000000011000 : out= 12'b000000011000;  12'b000000011001 : out= 12'b000000011001;  12'b000000011010 : out= 12'b000000011010;  12'b000000011011 : out= 12'b000000011011;  12'b000000011100 : out= 12'b000000011100;  12'b000000011101 : out= 12'b000000011101;  12'b000000011110 : out= 12'b000000011110;  12'b000000011111 : out= 12'b000000011111;  12'b000000100000 : out= 12'b000000100000;  12'b000000100001 : out= 12'b000000100001;  12'b000000100010 : out= 12'b000000100010;  12'b000000100011 : out= 12'b000000100011;  12'b000000100100 : out= 12'b000000100100;  12'b000000100101 : out= 12'b000000100101;  12'b000000100110 : out= 12'b000000100110;  12'b000000100111 : out= 12'b000000100111;  12'b000000101000 : out= 12'b000000101000;  12'b000000101001 : out= 12'b000000101001;  12'b000000101010 : out= 12'b000000101010;  12'b000000101011 : out= 12'b000000101011;  12'b000000101100 : out= 12'b000000101100;  12'b000000101101 : out= 12'b000000101101;  12'b000000101110 : out= 12'b000000101110;  12'b000000101111 : out= 12'b000000101111;  12'b000000110000 : out= 12'b000000110000;  12'b000000110001 : out= 12'b000000110001;  12'b000000110010 : out= 12'b000000110010;  12'b000000110011 : out= 12'b000000110011;  12'b000000110100 : out= 12'b000000110100;  12'b000000110101 : out= 12'b000000110101;  12'b000000110110 : out= 12'b000000110110;  12'b000000110111 : out= 12'b000000110111;  12'b000000111000 : out= 12'b000000111000;  12'b000000111001 : out= 12'b000000111001;  12'b000000111010 : out= 12'b000000111010;  12'b000000111011 : out= 12'b000000111011;  12'b000000111100 : out= 12'b000000111100;  12'b000000111101 : out= 12'b000000111101;  12'b000000111110 : out= 12'b000000111110;  12'b000000111111 : out= 12'b000000111111;  12'b000001000000 : out= 12'b000001000000;  12'b000001000001 : out= 12'b000001000001;  12'b000001000010 : out= 12'b000001000010;  12'b000001000011 : out= 12'b000001000011;  12'b000001000100 : out= 12'b000001000100;  12'b000001000101 : out= 12'b000001000101;  12'b000001000110 : out= 12'b000001000110;  12'b000001000111 : out= 12'b000001000111;  12'b000001001000 : out= 12'b000001001000;  12'b000001001001 : out= 12'b000001001001;  12'b000001001010 : out= 12'b000001001010;  12'b000001001011 : out= 12'b000001001011;  12'b000001001100 : out= 12'b000001001100;  12'b000001001101 : out= 12'b000001001101;  12'b000001001110 : out= 12'b000001001110;  12'b000001001111 : out= 12'b000001001111;  12'b000001010000 : out= 12'b000001010000;  12'b000001010001 : out= 12'b000001010001;  12'b000001010010 : out= 12'b000001010010;  12'b000001010011 : out= 12'b000001010011;  12'b000001010100 : out= 12'b000001010100;  12'b000001010101 : out= 12'b000001010101;  12'b000001010110 : out= 12'b000001010110;  12'b000001010111 : out= 12'b000001010111;  12'b000001011000 : out= 12'b000001011000;  12'b000001011001 : out= 12'b000001011001;  12'b000001011010 : out= 12'b000001011010;  12'b000001011011 : out= 12'b000001011011;  12'b000001011100 : out= 12'b000001011100;  12'b000001011101 : out= 12'b000001011101;  12'b000001011110 : out= 12'b000001011110;  12'b000001011111 : out= 12'b000001011111;  12'b000001100000 : out= 12'b000001100000;  12'b000001100001 : out= 12'b000001100001;  12'b000001100010 : out= 12'b000001100010;  12'b000001100011 : out= 12'b000001100011;  12'b000001100100 : out= 12'b000001100100;  12'b000001100101 : out= 12'b000001100101;  12'b000001100110 : out= 12'b000001100110;  12'b000001100111 : out= 12'b000001100111;  12'b000001101000 : out= 12'b000001101000;  12'b000001101001 : out= 12'b000001101001;  12'b000001101010 : out= 12'b000001101010;  12'b000001101011 : out= 12'b000001101011;  12'b000001101100 : out= 12'b000001101100;  12'b000001101101 : out= 12'b000001101101;  12'b000001101110 : out= 12'b000001101110;  12'b000001101111 : out= 12'b000001101111;  12'b000001110000 : out= 12'b000001110000;  12'b000001110001 : out= 12'b000001110001;  12'b000001110010 : out= 12'b000001110010;  12'b000001110011 : out= 12'b000001110011;  12'b000001110100 : out= 12'b000001110100;  12'b000001110101 : out= 12'b000001110101;  12'b000001110110 : out= 12'b000001110110;  12'b000001110111 : out= 12'b000001110111;  12'b000001111000 : out= 12'b000001111000;  12'b000001111001 : out= 12'b000001111001;  12'b000001111010 : out= 12'b000001111010;  12'b000001111011 : out= 12'b000001111011;  12'b000001111100 : out= 12'b000001111100;  12'b000001111101 : out= 12'b000001111101;  12'b000001111110 : out= 12'b000001111110;  12'b000001111111 : out= 12'b000001111111;  12'b000010000000 : out= 12'b000010000000;  12'b000010000001 : out= 12'b000010000001;  12'b000010000010 : out= 12'b000010000010;  12'b000010000011 : out= 12'b000010000011;  12'b000010000100 : out= 12'b000010000100;  12'b000010000101 : out= 12'b000010000101;  12'b000010000110 : out= 12'b000010000110;  12'b000010000111 : out= 12'b000010000111;  12'b000010001000 : out= 12'b000010001000;  12'b000010001001 : out= 12'b000010001001;  12'b000010001010 : out= 12'b000010001010;  12'b000010001011 : out= 12'b000010001011;  12'b000010001100 : out= 12'b000010001100;  12'b000010001101 : out= 12'b000010001101;  12'b000010001110 : out= 12'b000010001110;  12'b000010001111 : out= 12'b000010001111;  12'b000010010000 : out= 12'b000010010000;  12'b000010010001 : out= 12'b000010010001;  12'b000010010010 : out= 12'b000010010010;  12'b000010010011 : out= 12'b000010010011;  12'b000010010100 : out= 12'b000010010100;  12'b000010010101 : out= 12'b000010010101;  12'b000010010110 : out= 12'b000010010110;  12'b000010010111 : out= 12'b000010010111;  12'b000010011000 : out= 12'b000010011000;  12'b000010011001 : out= 12'b000010011001;  12'b000010011010 : out= 12'b000010011010;  12'b000010011011 : out= 12'b000010011011;  12'b000010011100 : out= 12'b000010011100;  12'b000010011101 : out= 12'b000010011101;  12'b000010011110 : out= 12'b000010011110;  12'b000010011111 : out= 12'b000010011111;  12'b000010100000 : out= 12'b000010100000;  12'b000010100001 : out= 12'b000010100001;  12'b000010100010 : out= 12'b000010100010;  12'b000010100011 : out= 12'b000010100011;  12'b000010100100 : out= 12'b000010100100;  12'b000010100101 : out= 12'b000010100101;  12'b000010100110 : out= 12'b000010100110;  12'b000010100111 : out= 12'b000010100111;  12'b000010101000 : out= 12'b000010101000;  12'b000010101001 : out= 12'b000010101001;  12'b000010101010 : out= 12'b000010101010;  12'b000010101011 : out= 12'b000010101011;  12'b000010101100 : out= 12'b000010101100;  12'b000010101101 : out= 12'b000010101101;  12'b000010101110 : out= 12'b000010101110;  12'b000010101111 : out= 12'b000010101111;  12'b000010110000 : out= 12'b000010110000;  12'b000010110001 : out= 12'b000010110001;  12'b000010110010 : out= 12'b000010110010;  12'b000010110011 : out= 12'b000010110011;  12'b000010110100 : out= 12'b000010110100;  12'b000010110101 : out= 12'b000010110101;  12'b000010110110 : out= 12'b000010110110;  12'b000010110111 : out= 12'b000010110111;  12'b000010111000 : out= 12'b000010111000;  12'b000010111001 : out= 12'b000010111001;  12'b000010111010 : out= 12'b000010111010;  12'b000010111011 : out= 12'b000010111011;  12'b000010111100 : out= 12'b000010111100;  12'b000010111101 : out= 12'b000010111101;  12'b000010111110 : out= 12'b000010111110;  12'b000010111111 : out= 12'b000010111111;  12'b000011000000 : out= 12'b000011000000;  12'b000011000001 : out= 12'b000011000001;  12'b000011000010 : out= 12'b000011000010;  12'b000011000011 : out= 12'b000011000011;  12'b000011000100 : out= 12'b000011000100;  12'b000011000101 : out= 12'b000011000101;  12'b000011000110 : out= 12'b000011000110;  12'b000011000111 : out= 12'b000011000111;  12'b000011001000 : out= 12'b000011001000;  12'b000011001001 : out= 12'b000011001001;  12'b000011001010 : out= 12'b000011001010;  12'b000011001011 : out= 12'b000011001011;  12'b000011001100 : out= 12'b000011001100;  12'b000011001101 : out= 12'b000011001101;  12'b000011001110 : out= 12'b000011001110;  12'b000011001111 : out= 12'b000011001111;  12'b000011010000 : out= 12'b000011010000;  12'b000011010001 : out= 12'b000011010001;  12'b000011010010 : out= 12'b000011010010; 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 12'b111101011011 : out= 12'b111101011011;  12'b111101011100 : out= 12'b111101011100;  12'b111101011101 : out= 12'b111101011101;  12'b111101011110 : out= 12'b111101011110;  12'b111101011111 : out= 12'b111101011111;  12'b111101100000 : out= 12'b111101100000;  12'b111101100001 : out= 12'b111101100001;  12'b111101100010 : out= 12'b111101100010;  12'b111101100011 : out= 12'b111101100011;  12'b111101100100 : out= 12'b111101100100;  12'b111101100101 : out= 12'b111101100101;  12'b111101100110 : out= 12'b111101100110;  12'b111101100111 : out= 12'b111101100111;  12'b111101101000 : out= 12'b111101101000;  12'b111101101001 : out= 12'b111101101001;  12'b111101101010 : out= 12'b111101101010;  12'b111101101011 : out= 12'b111101101011;  12'b111101101100 : out= 12'b111101101100;  12'b111101101101 : out= 12'b111101101101;  12'b111101101110 : out= 12'b111101101110;  12'b111101101111 : out= 12'b111101101111;  12'b111101110000 : out= 12'b111101110000;  12'b111101110001 : out= 12'b111101110001;  12'b111101110010 : out= 12'b111101110010;  12'b111101110011 : out= 12'b111101110011;  12'b111101110100 : out= 12'b111101110100;  12'b111101110101 : out= 12'b111101110101;  12'b111101110110 : out= 12'b111101110110;  12'b111101110111 : out= 12'b111101110111;  12'b111101111000 : out= 12'b111101111000;  12'b111101111001 : out= 12'b111101111001;  12'b111101111010 : out= 12'b111101111010;  12'b111101111011 : out= 12'b111101111011;  12'b111101111100 : out= 12'b111101111100;  12'b111101111101 : out= 12'b111101111101;  12'b111101111110 : out= 12'b111101111110;  12'b111101111111 : out= 12'b111101111111;  12'b111110000000 : out= 12'b111110000000;  12'b111110000001 : out= 12'b111110000001;  12'b111110000010 : out= 12'b111110000010;  12'b111110000011 : out= 12'b111110000011;  12'b111110000100 : out= 12'b111110000100;  12'b111110000101 : out= 12'b111110000101;  12'b111110000110 : out= 12'b111110000110;  12'b111110000111 : out= 12'b111110000111;  12'b111110001000 : out= 12'b111110001000;  12'b111110001001 : out= 12'b111110001001;  12'b111110001010 : out= 12'b111110001010;  12'b111110001011 : out= 12'b111110001011;  12'b111110001100 : out= 12'b111110001100;  12'b111110001101 : out= 12'b111110001101;  12'b111110001110 : out= 12'b111110001110;  12'b111110001111 : out= 12'b111110001111;  12'b111110010000 : out= 12'b111110010000;  12'b111110010001 : out= 12'b111110010001;  12'b111110010010 : out= 12'b111110010010;  12'b111110010011 : out= 12'b111110010011;  12'b111110010100 : out= 12'b111110010100;  12'b111110010101 : out= 12'b111110010101;  12'b111110010110 : out= 12'b111110010110;  12'b111110010111 : out= 12'b111110010111;  12'b111110011000 : out= 12'b111110011000;  12'b111110011001 : out= 12'b111110011001;  12'b111110011010 : out= 12'b111110011010;  12'b111110011011 : out= 12'b111110011011;  12'b111110011100 : out= 12'b111110011100;  12'b111110011101 : out= 12'b111110011101;  12'b111110011110 : out= 12'b111110011110;  12'b111110011111 : out= 12'b111110011111;  12'b111110100000 : out= 12'b111110100000;  12'b111110100001 : out= 12'b111110100001;  12'b111110100010 : out= 12'b111110100010;  12'b111110100011 : out= 12'b111110100011;  12'b111110100100 : out= 12'b111110100100;  12'b111110100101 : out= 12'b111110100101;  12'b111110100110 : out= 12'b111110100110;  12'b111110100111 : out= 12'b111110100111;  12'b111110101000 : out= 12'b111110101000;  12'b111110101001 : out= 12'b111110101001;  12'b111110101010 : out= 12'b111110101010;  12'b111110101011 : out= 12'b111110101011;  12'b111110101100 : out= 12'b111110101100;  12'b111110101101 : out= 12'b111110101101;  12'b111110101110 : out= 12'b111110101110;  12'b111110101111 : out= 12'b111110101111;  12'b111110110000 : out= 12'b111110110000;  12'b111110110001 : out= 12'b111110110001;  12'b111110110010 : out= 12'b111110110010;  12'b111110110011 : out= 12'b111110110011;  12'b111110110100 : out= 12'b111110110100;  12'b111110110101 : out= 12'b111110110101;  12'b111110110110 : out= 12'b111110110110;  12'b111110110111 : out= 12'b111110110111;  12'b111110111000 : out= 12'b111110111000;  12'b111110111001 : out= 12'b111110111001;  12'b111110111010 : out= 12'b111110111010;  12'b111110111011 : out= 12'b111110111011;  12'b111110111100 : out= 12'b111110111100;  12'b111110111101 : out= 12'b111110111101;  12'b111110111110 : out= 12'b111110111110;  12'b111110111111 : out= 12'b111110111111;  12'b111111000000 : out= 12'b111111000000;  12'b111111000001 : out= 12'b111111000001;  12'b111111000010 : out= 12'b111111000010;  12'b111111000011 : out= 12'b111111000011;  12'b111111000100 : out= 12'b111111000100;  12'b111111000101 : out= 12'b111111000101;  12'b111111000110 : out= 12'b111111000110;  12'b111111000111 : out= 12'b111111000111;  12'b111111001000 : out= 12'b111111001000;  12'b111111001001 : out= 12'b111111001001;  12'b111111001010 : out= 12'b111111001010;  12'b111111001011 : out= 12'b111111001011;  12'b111111001100 : out= 12'b111111001100;  12'b111111001101 : out= 12'b111111001101;  12'b111111001110 : out= 12'b111111001110;  12'b111111001111 : out= 12'b111111001111;  12'b111111010000 : out= 12'b111111010000;  12'b111111010001 : out= 12'b111111010001;  12'b111111010010 : out= 12'b111111010010;  12'b111111010011 : out= 12'b111111010011;  12'b111111010100 : out= 12'b111111010100;  12'b111111010101 : out= 12'b111111010101;  12'b111111010110 : out= 12'b111111010110;  12'b111111010111 : out= 12'b111111010111;  12'b111111011000 : out= 12'b111111011000;  12'b111111011001 : out= 12'b111111011001;  12'b111111011010 : out= 12'b111111011010;  12'b111111011011 : out= 12'b111111011011;  12'b111111011100 : out= 12'b111111011100;  12'b111111011101 : out= 12'b111111011101;  12'b111111011110 : out= 12'b111111011110;  12'b111111011111 : out= 12'b111111011111;  12'b111111100000 : out= 12'b111111100000;  12'b111111100001 : out= 12'b111111100001;  12'b111111100010 : out= 12'b111111100010;  12'b111111100011 : out= 12'b111111100011;  12'b111111100100 : out= 12'b111111100100;  12'b111111100101 : out= 12'b111111100101;  12'b111111100110 : out= 12'b111111100110;  12'b111111100111 : out= 12'b111111100111;  12'b111111101000 : out= 12'b111111101000;  12'b111111101001 : out= 12'b111111101001;  12'b111111101010 : out= 12'b111111101010;  12'b111111101011 : out= 12'b111111101011;  12'b111111101100 : out= 12'b111111101100;  12'b111111101101 : out= 12'b111111101101;  12'b111111101110 : out= 12'b111111101110;  12'b111111101111 : out= 12'b111111101111;  12'b111111110000 : out= 12'b111111110000;  12'b111111110001 : out= 12'b111111110001;  12'b111111110010 : out= 12'b111111110010;  12'b111111110011 : out= 12'b111111110011;  12'b111111110100 : out= 12'b111111110100;  12'b111111110101 : out= 12'b111111110101;  12'b111111110110 : out= 12'b111111110110;  12'b111111110111 : out= 12'b111111110111;  12'b111111111000 : out= 12'b111111111000;  12'b111111111001 : out= 12'b111111111001;  12'b111111111010 : out= 12'b111111111010;  12'b111111111011 : out= 12'b111111111011;  12'b111111111100 : out= 12'b111111111100;  12'b111111111101 : out= 12'b111111111101;  12'b111111111110 : out= 12'b111111111110;  12'b111111111111 : out= 12'b111111111111;  endcase  end  endmodule |

**RTL:**

Finally our RTL View (in closed shape) are presented below: